CLAIMS:

1. A method for the manufacture of a semiconductor device containing a field-effect transistor with a gate electrode (1), a source region (2) and a drain region (3), wherein a gate oxide layer (4) is formed on a surface of a semiconductor body (10) of silicon, on which gate oxide layer the gate electrode (1) containing a polycrystalline silicon layer (1) is provided locally, wherein the source region (2) and the drain region (3) are formed, in the semiconductor body (10), on both sides of the gate electrode (1) and a part (3A) of the drain region (3) bordering the gate electrode (1) is provided with a lower doping concentration, and wherein a spacer (5) of a material that can be selectively etched with respect to the gate oxide layer (4), is produced on both sides of the gate electrode (1), characterised in that for the formation of the drain region (3) and the lowly doped part (3A) thereof, two additional mask in layers (6,7) are deposited on the surface of the semiconductor body (10), the drain region (3) being formed at a distance from the gate electrode (1) that is larger than the width of the spacer (5).

2. A method as claimed in claim 1, characterised in that for the formation of the lowly doped part (3A) of the drain region (3) a first masking layer (6) extending so far as to be on the gate electrode (1) is produced on the side of the gate electrode (1) of the source region (2) to be formed on the surface of the semiconductor body (10), and a second masking layer (7) extending from the gate electrode (1) up to the drain region (3) to be formed is produced on the surface of the semiconductor body (10).

3. A method as claimed in claim 1 or 2, characterised in that at the location of the source region (2) and the drain region (3) the gate oxide layer (4) is provided with an aperture (8,9) and that at the location of the aperture (8,9) the gate electrode (1) and the source region (2) and the drain region (3) are provided with a metal layer (11), which with the aid of the underlying silicon is converted into a silicide layer (11).

4. A method as claimed in claim 1, 2 or 3, characterised in that the distance from the drain region (3) to the gate electrode (1) is chosen between 1 and 4 μm.

5. A method as claimed in anyone of the above claims, characterised in that on the gate electrode (1) an isolating layer (26) is deposited, on which a shielding electrode (27) is produced at the location of the gate electrode (1).

6. A method as claimed in anyone of the above claims, characterised in that the spacers (5) are formed of a layer (5A) of silicon nitride.

7. A method as claimed in anyone of the above claims, characterised in that the spacers (5) are formed of a layer of silicon nitride (5A) on which a layer (5B) of polycrystalline silicon is deposited.

8. A method as claimed in anyone of the above claims, characterised in that additional semiconductor elements and preferably one or more passive components are integrated into the semiconductor body (10).

9. A semiconductor device comprising a field-effect transistor obtained by means of a method as claimed in anyone of the above claims.